



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,726	11/09/2001	Chung-Ching Lai	0941-0363P-SP	5867

2292 7590 05/28/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

OWENS, DOUGLAS W

ART UNIT PAPER NUMBER

2811

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/986,726

Applicant(s)

LAI ET AL.

Examiner

Douglas W Owens

Art Unit

2811

pmw

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11/09/01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/09/01.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the invention of group II in the paper filed on April 19, 2004 is acknowledged. The traversal is on the ground(s) that it should be no undue burden on the Examiner to consider both inventions. This is not found persuasive because the assertion that it should be no undue burden to search both inventions is merely speculative.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 5 – 11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,652,156 to Liao et al.

Regarding claim 5, Liao et al. teach a method of forming a gate for preventing dopants from penetrating a gate insulator, the method comprising:

providing a substrate (10);

forming a gate insulator (12) on the substrate;

forming a polysilicon layer (22; Col. 2, line 67 – Col. 3, line 2);

forming an amorphous silicon layer (24; Col. 3, lines 7 – 9) on the polysilicon layer;

patterning the polysilicon layer and the amorphous silicon layer to form a gate (Figs. 7 and 8; Col. 3, lines 20 – 23).

Regarding claim 6, Liao et al. teach a method, wherein the gate insulator is a gate oxide layer (Col. 2, lines 42 – 44).

Regarding claim 7, Liao et al. teach a method, wherein the thickness of the polysilicon layer is 1000 Angstroms (Col. 2, line 67 – Col. 3, line 2), which is within the claimed range.

Regarding claim 8, Liao et al. teach a method, wherein forming the polysilicon layer comprises using silane as a processing gas (Col. 2, lines 57 – 59), under a pressure of 0.2 to 0.3 Torr (Col. 2, lines 59 – 61) at 620° to 650° Celsius (Col. 2, lines 51 and 52), both ranges include portions inside the claimed ranges of 0.15 – 0.25 Torr and 580° to 630° C.

Regarding claim 9, Liao et al. teach a method, wherein the thickness of the amorphous silicon layer is 200 to 1000 Angstroms (Col. 2, lines 62 – 64; Col. 3, lines 14 and 15; *Note that layers are repeated alternately)

Regarding claim 10, Liao et al. teach a method, wherein forming the amorphous silicon layer comprises using silane as a processing gas (Col. 2, lines 55 – 57) at a pressure of 0.2 – 0.3 Torr (Col. 2, lines 59 – 61) at 480° to 510° Celsius (Col. 2, lines 48

– 50), both ranges include portion inside the claimed ranges of 0.15 – 0.25 Torr and 510° to 560° C.

Regarding claims 11 and 13, Liao et al. teach a method, wherein after the step of patterning the gate, a source/drain layer is formed in the substrate by boron ion implantation (Col. 3, lines 24 – 27).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. as applied to claims 5 and 11 above, and further in view of Admitted Prior Art.

Regarding claim 12, Liao et al. do not teach a method, wherein after performing the ion implantation, an anneal process is performed. Admitted Prior Art teaches performing an anneal step after implanting boron ions (Page 1, line 27 – Page 2, line 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform an anneal step after the boron implant, since it is desirable to activate the dopants, as well as repair substrate damage.

7. Claims 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liao et al. as applied to claims 5, 11 and 13 above, and further in view of US Patent No. 6,740,912 to Chaudhry et al.

Regarding claim 14, Liao et al. do not teach an boron implant energy in the range of 3 – 20 keV or a dose in the range of $1 \times 10^{15}/\text{cm}^2$ – $1 \times 10^{16}/\text{cm}^2$. Indeed, Liao et al. is silent with respect to the implant dosage and energy. Chaudhry et al. teach a boron source/drain implant dosage in the range of 0.5 – 10 keV, and a dosage in the range of $5 \times 10^{14}/\text{cm}^2$ – $5 \times 10^{15}/\text{cm}^2$ (Col. 4, lines 25 – 29), both ranges overlapping the claimed range. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method taught by Chaudhry et al. into the method taught by Liao et al., since it is desirable to use reliable methods of forming source/drain regions.

Regarding claim 15, Liao et al. teaches a method that may be applied to form an N channel MOSFET (Fig. 8; Col. 3, lines 43 – 48). Liao et al. does not teach a method, wherein arsenic is the dopant used in the implant process. Liao et al. is silent with respect to the dopant used, and one having ordinary skill in the art would be required to select a dopant that can be used for an N channel MOSFET. Chaudhry et al. teach a method, wherein an N channel MOSFET is formed by using an arsenic implant in the source/drain regions (Col. 4, lines 21 – 25). It would have been obvious to one of ordinary skill in the art to incorporate the method taught by Chaudhry et al. into the method of Liao et al., since it is desirable to select reliable materials in the formation of N channel MOSFETs.

Regarding claim 16, Liao et al. do not teach an arsenic implant energy in the range of 30 – 80 keV or a dose in the range of $1 \times 10^{15}/\text{cm}^2$ – $1 \times 10^{16}/\text{cm}^2$. Indeed, Liao et al. is silent with respect to the implant dosage and energy. Chaudhry et al. teach an

Art Unit: 2811

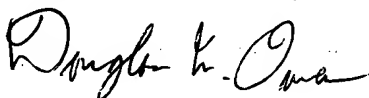
arsenic source/drain implant dosage in the range of 5 – 50 keV, and a dosage in the range of $5 \times 10^{14}/\text{cm}^2$ – $5 \times 10^{15}/\text{cm}^2$ (Col. 4, lines 21 – 25) both ranges overlapping the claimed range. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method taught by Chaudhry et al. into the method taught by Liao et al., since it is desirable to use reliable methods of forming source/drain regions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas W. Owens
Patent Examiner